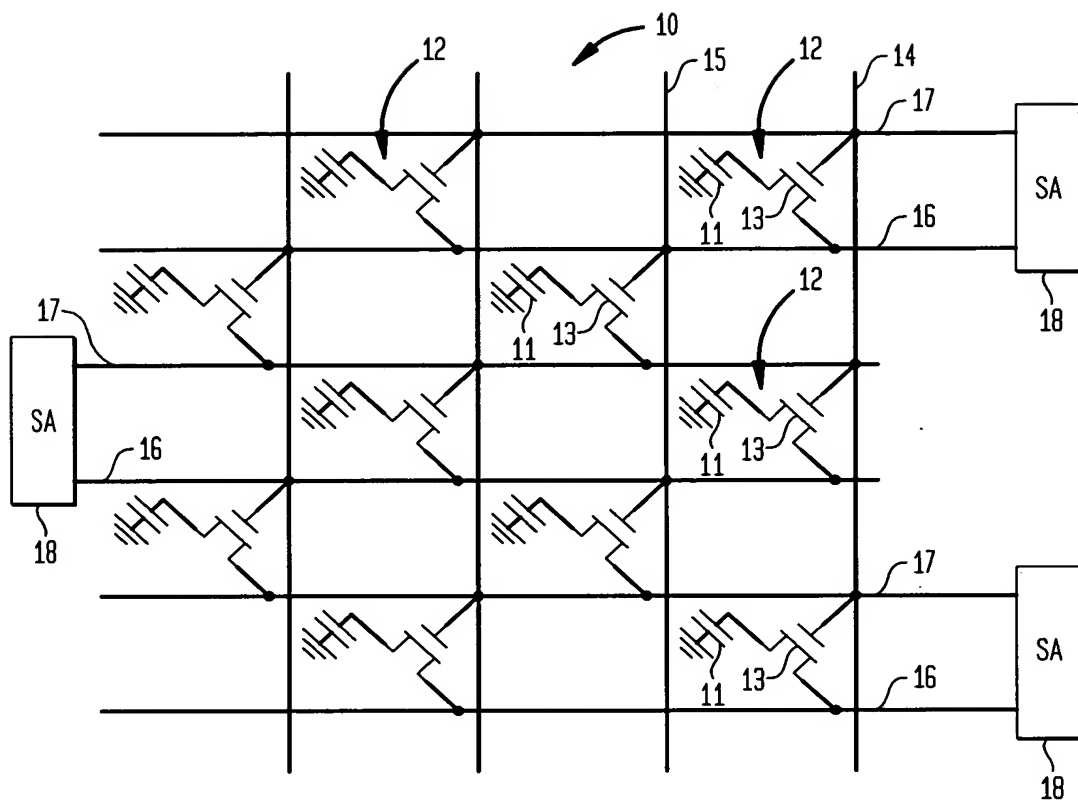


FIG. 1A
(PRIOR ART)



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FIG. 1B

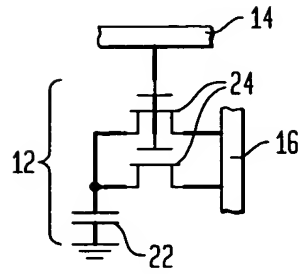
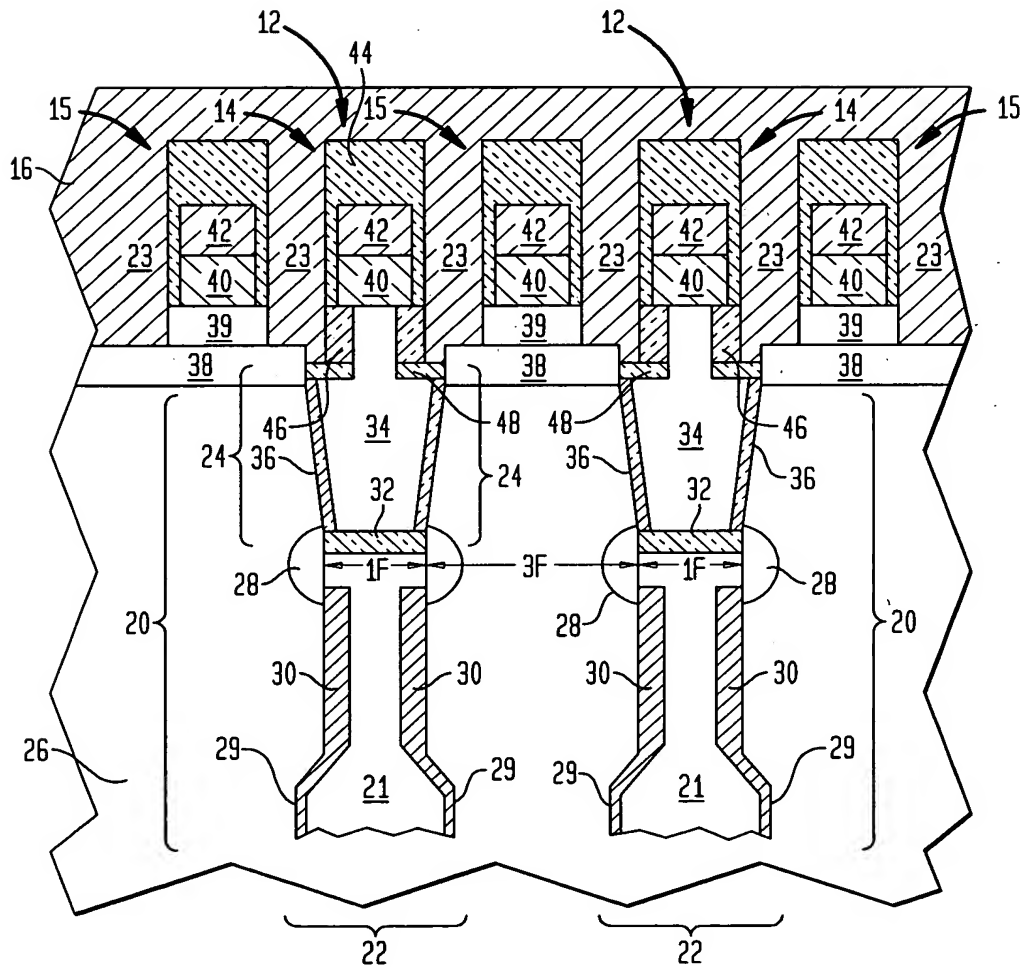


FIG. 1C



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FIG. 2A

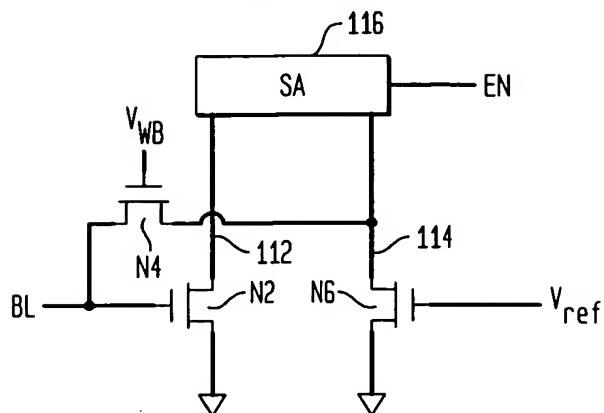


FIG. 2B

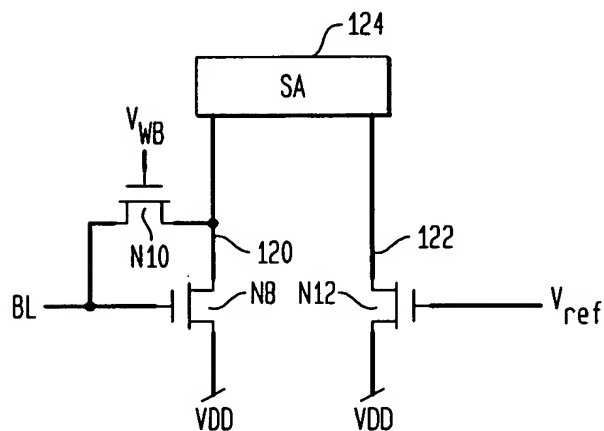


FIG. 2C

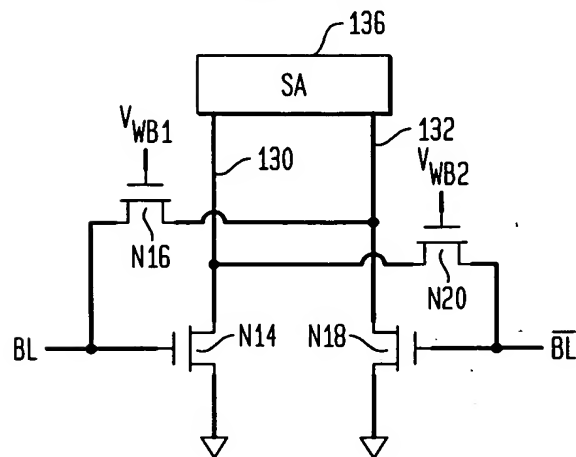
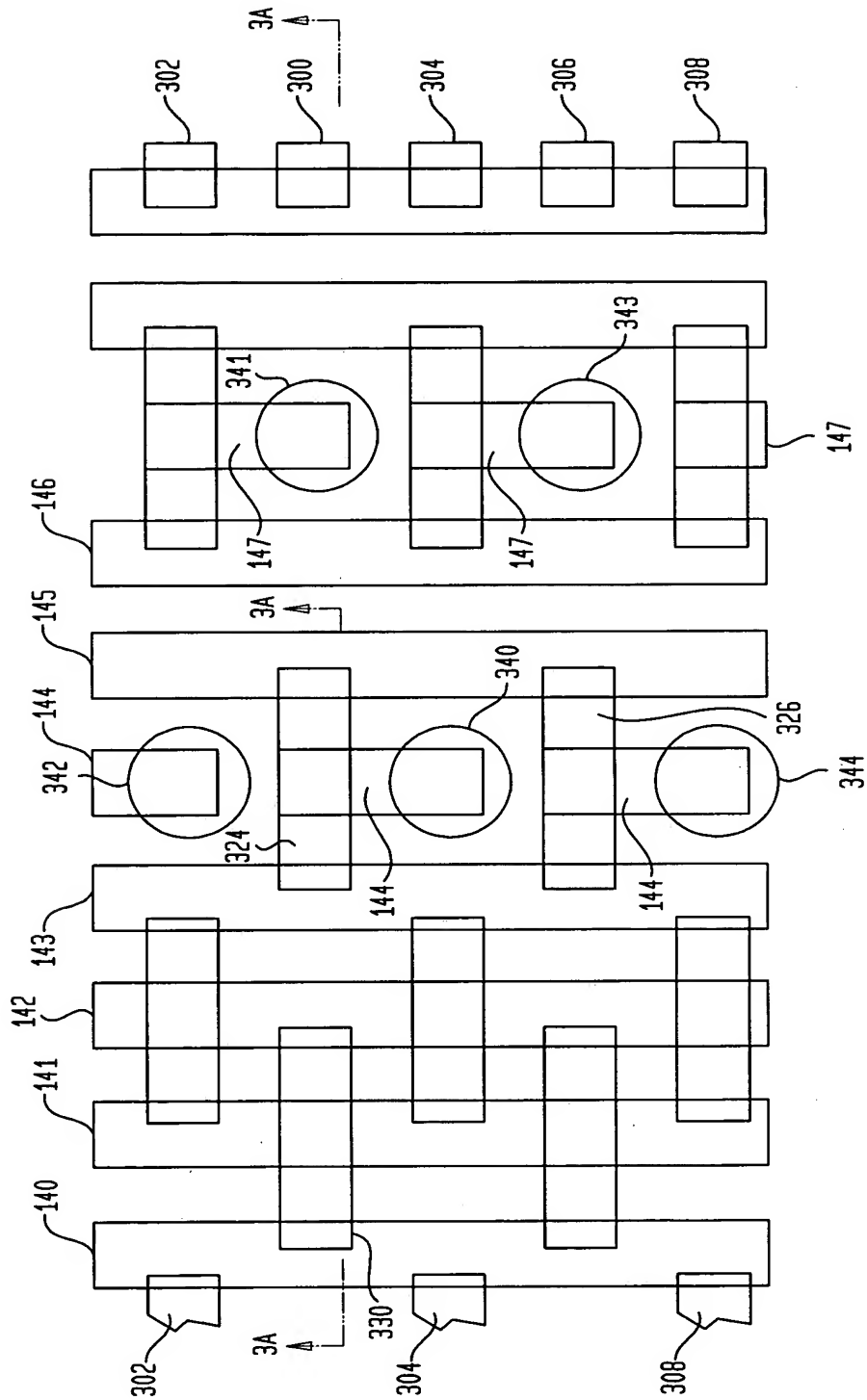


FIG. 3A

FIG. 3A is a cross-sectional view of a semiconductor device. The device includes a substrate 300 with a series of vertical structures 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100. The structures are arranged in a row and are connected to a common line 300. The structures are labeled with various reference numerals indicating different layers and features.

FIG. 3B



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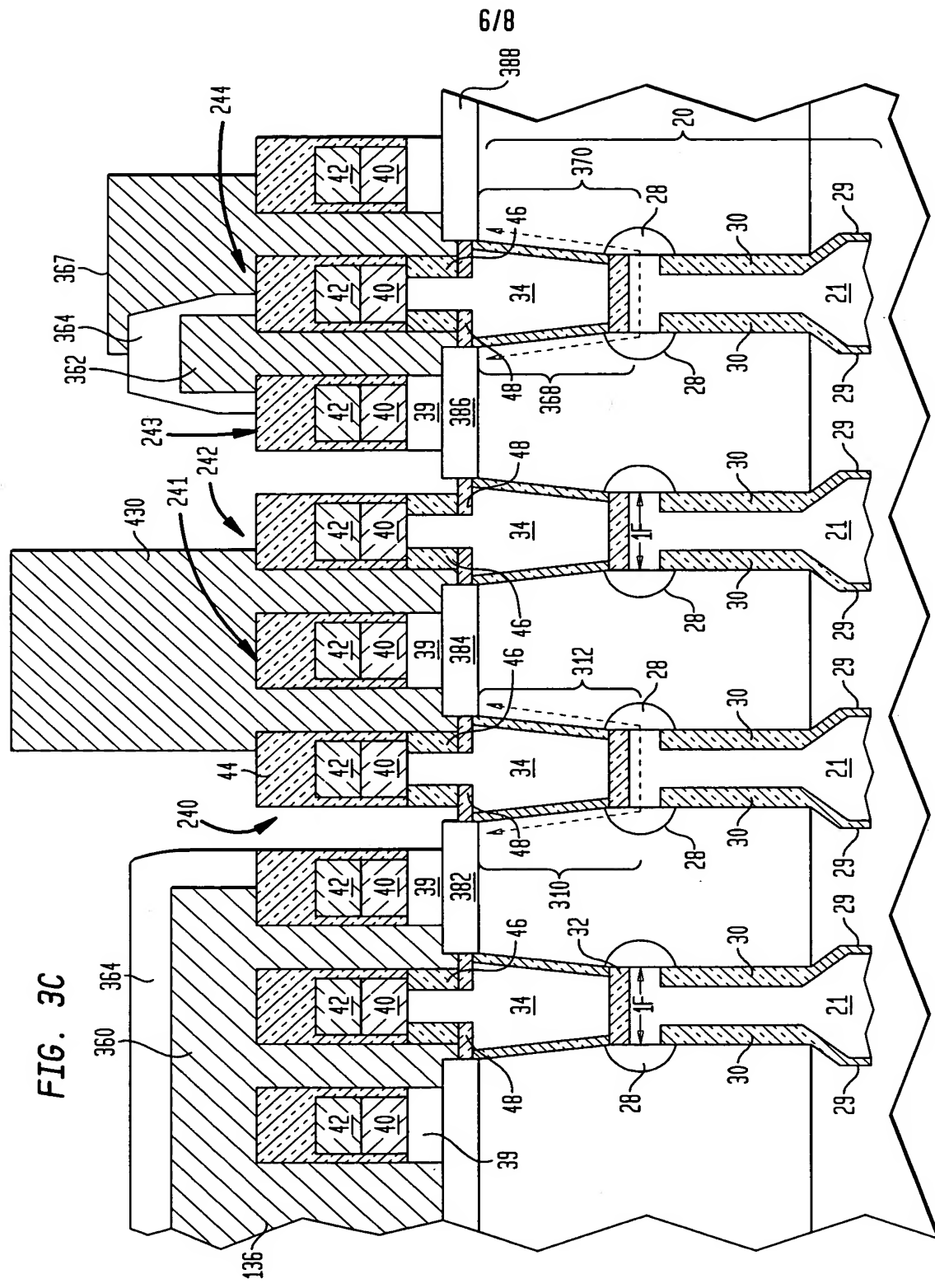


FIG. 3C

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FIG. 4A

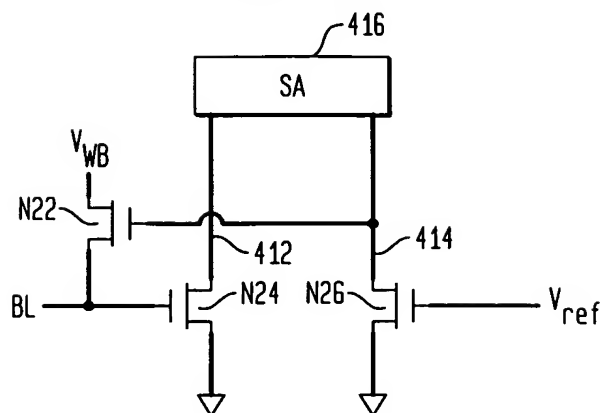


FIG. 4B

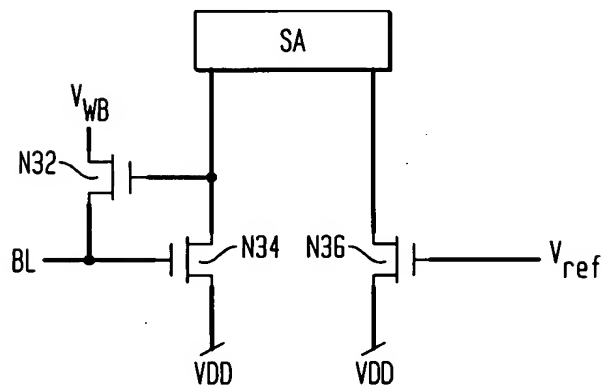


FIG. 4C

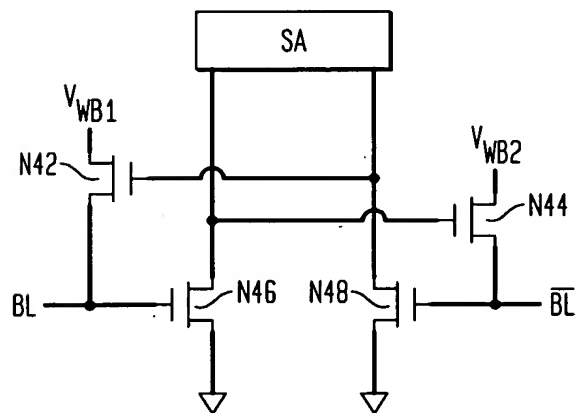


FIG. 5A

